FE-H Status

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Organization of Basic Tasks:

- What they are and who is doing them.

Status:

- Quick overview of present status, highlighting recent progress on digital readout circuitry at LBL (Marchesini and Mandelli).

Next step:

- Hold 3-day workshop next week at CERN with Bonn, CPPM, LBL working together to go through present status and remaining issues.

Gerrit will give separate talk on details of his work on FE-H.

Organization

Basic Tasks for FE-H:

- **Front-end design:** preamplifier and discriminator.
- **Miscellaneous analog cells:** current and voltage DACs, current references, VCCD/VTH amplifiers, FE bias generation cells, LVDS drivers and receivers, and calibration chopper.
- **Control logic:** command decoder, global register, pixel register, pixel control logic, hitbus OR tree, column mask logic, output MUXes.
- **Pixel readout logic:** hit logic, LE/TE RAMs, address ROMs.
- **Bottom of column logic:** sense amplifiers and CEU logic plus buffering.
- **End of column logic:** EOC buffers, horizontal sparse scan, plus buffering.
- **Peripheral digital logic:** grey generator, reset generator, clock generators, self-trigger logic, readout control logic, trigger FIFO, TOT subtractor, serializer.
- **Overall integration and floorplanning**: placing all blocks, routing all interconnects, and assessing global signal distribution issues.

Status

Overall:

- Layout rules and technology file are finalized for HSOI4 with Cadence 4.4. Gerrit also received Dracula rules and has run his standard cell library through these checks (DIVA rules for HSOI are not quite complete, so some additional errors can appear).
- Gerrit has completed and characterized his Standard Cell library, and has implemented the “back-annotated Verilog” approach that he wants to use to give higher quality timing results. He intends to use automatic place and route for non-critical circuit blocks where possible (control logic and digital peripheral logic) to accelerate schedule.
- We have moved to Cadence release 4.4.2 (including installation of the new DMILL design kit which only works under 4.4). We have purchased one license, and will soon get another one, for the ELDO simulation environment for Cadence 4.4 (the so-called OASIS Simulation environment).

Front-end Design:

- Laurent has been working seriously. He has reviewed and updated the BSIM3 models for operation with ELDO. We agreed on a first approach for the post-rad corners, and updated models exist.
- He has studied the PMOS and NMOS characteristics, and understands relatively well how the process is built. He is presently modifying the FE-D design to optimize the performance in HSOI, and is performing extensive simulations to back up this updated design. Possible changes include an NMOS input device with a straight cascode instead of a PMOS with folded cascode, potentially leading to better timewalk performance.

Analog Cells:

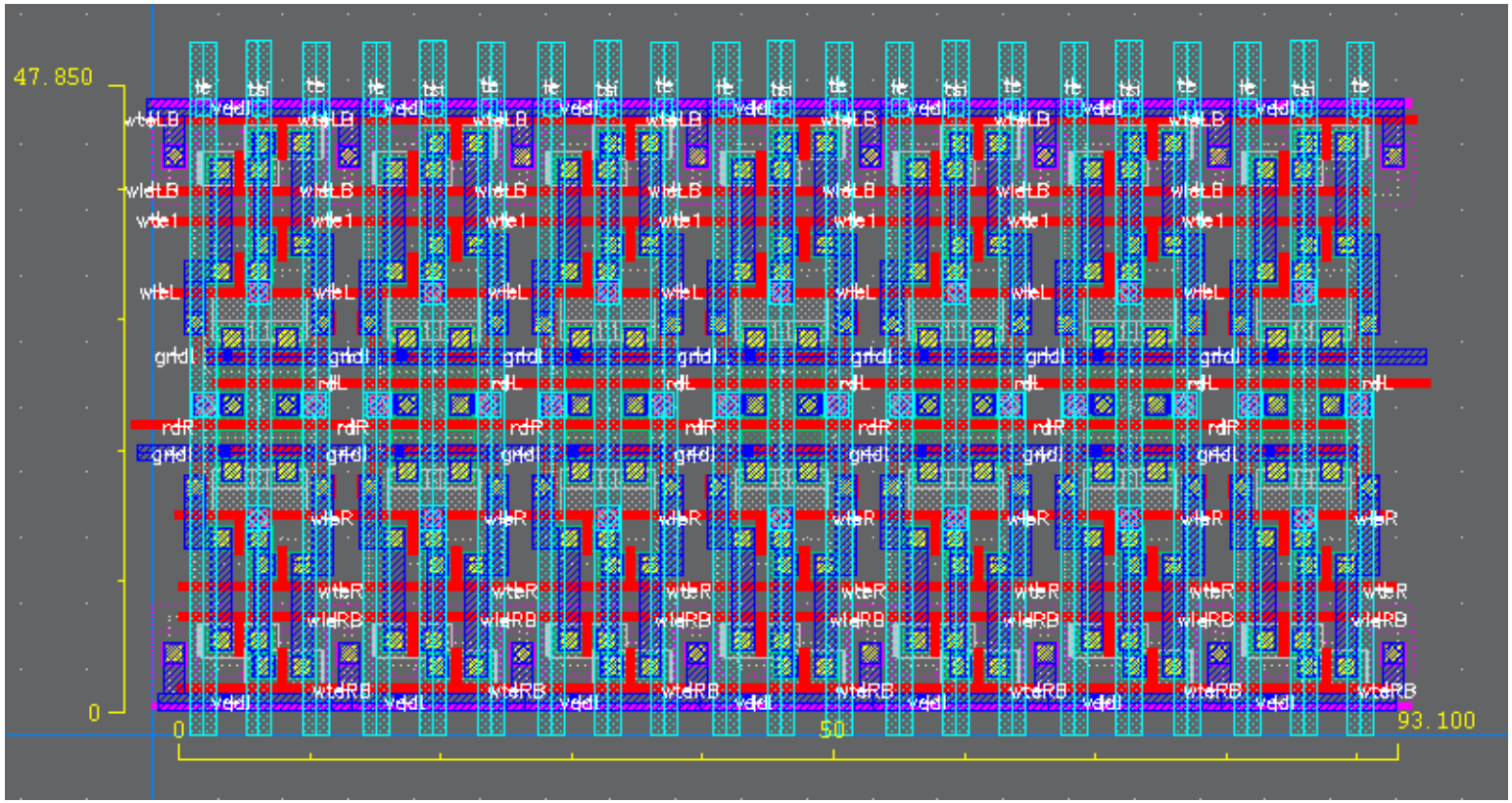
- For FE-D, these were designed by Laurent and Peter. There are several minor conversion issues to look at, including a CMOS current reference. The first step would be to have the original designers re-simulate the blocks at the schematic level using HSOI models. Then, depending on resources available at Bonn and LBL, the work would be shared in some manner.
- This is the major area where we hope for Bonn involvement in the near future.

Control Logic:

- For the control logic in the pixel, a first pass design and layout has been done by Emanuele. It is conceptually similar to FE-D, but one extra control FF has been added, which could be used for disabling preamplifiers, or other diagnostic roles.
- The first pass was based on the standard cells of Gerrit, which use a very conservative latch and FF design. The resulting control block is larger than the one of FE-D (it is about 110μ long, in contrast to the 90μ used for FE-D). We believe a custom version, using less conservative cells (but still fully static), would be about 60μ long.
- With the present readout logic size, this would leave about 130μ left for the front-end circuitry in order to acheive the 300μ pitch. This looks quite plausible.
- Once the bottom of column layout for the readout is complete, Emanuele will return to the pixel control logic, and also do the layout for the control logic that goes in the bottom of column (column enable logic).
- There are several blocks in this category which are placed in the bottom of the chip, including the command decoder, the output MUXes, and parts of the Global Register. These blocks will most likely be done by Gerrit as he assembles the bottom of the chip, and might be synthesized directly from the Verilog.

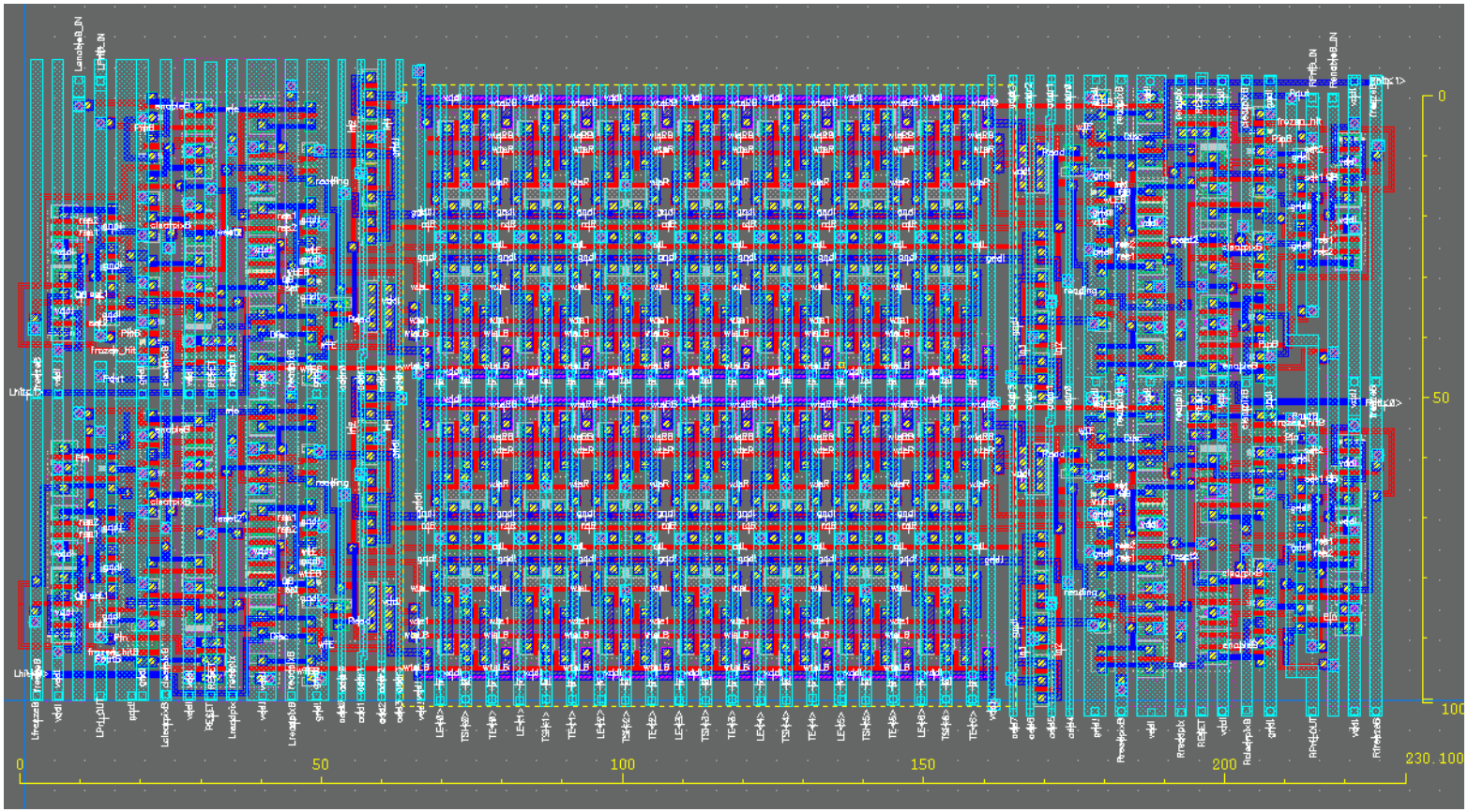
Pixel Readout and CEU Logic:

- Emanuele has been working on this. He has improved the hit logic in the pixel to eliminate all significant multi-hit problems (only remaining problem is when a second hit overlaps the 12.5ns wide ClearPix signal). The new logic still uses a dynamic FF, but its design has been improved. The new RAM cell design has also been improved with a transmission gate and NMOS instead of PMOS:



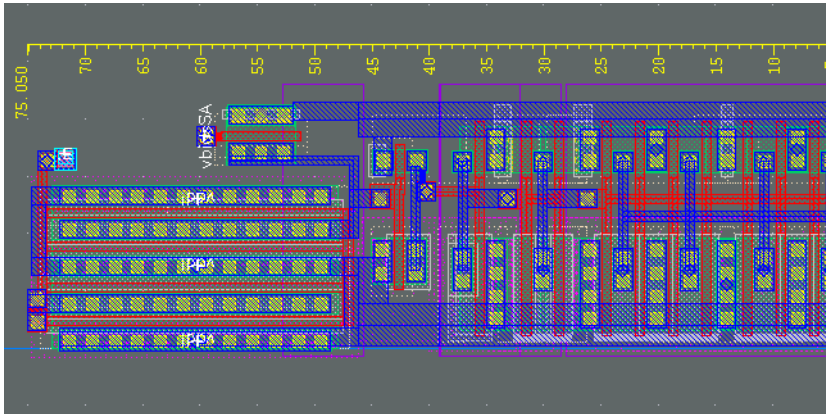
- The figure shows the layout of the pair of 7-bit RAM cells used for LE/TE latches.

- A layout of the full DigCol2x16 block has been done, with the second generation of layout for the hit logic. The new size is about 230µ pitch, compared to the 274µ use for FE-D.
- The figure shows the layout for the basic 2x2 building block of the digital readout:

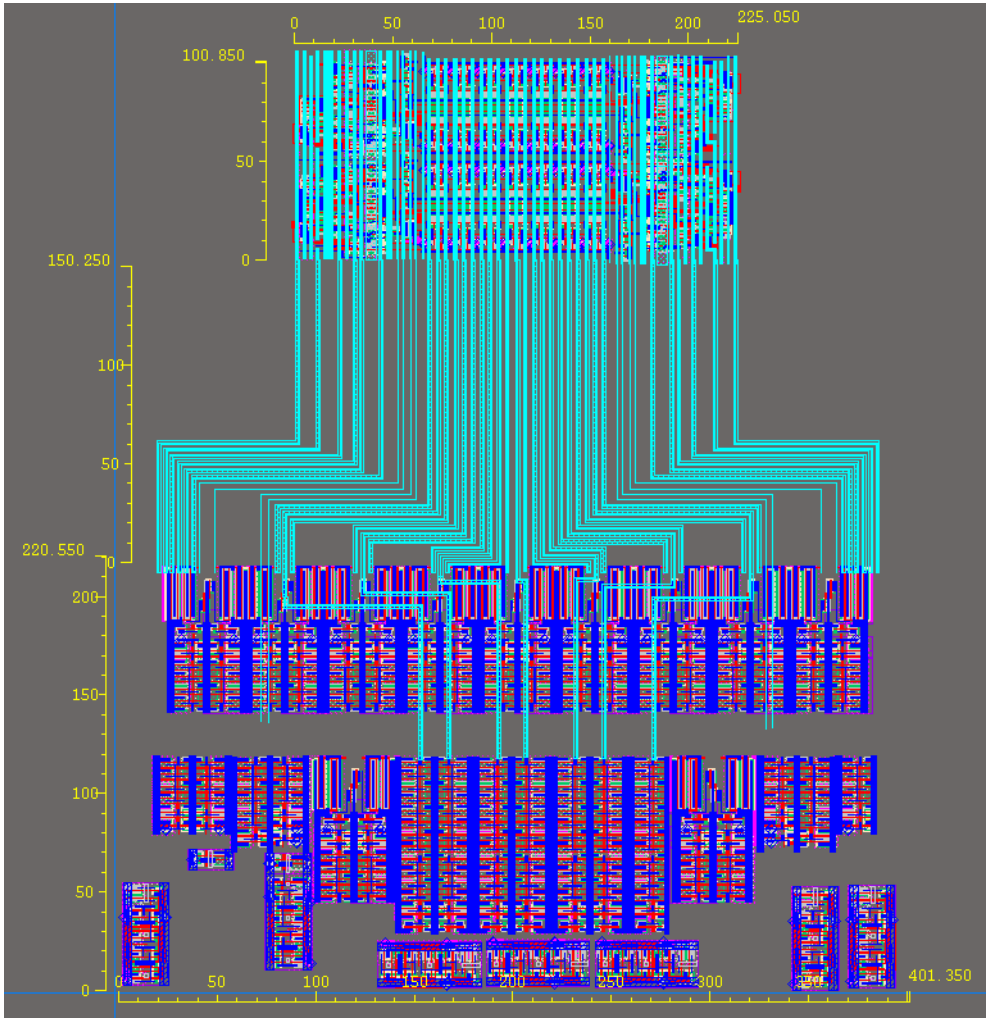


Significant work has been done on the CEU region as well:

- An improved CEU design was done, eliminating some of the timing problems of the design used in FE-D.
- We decided to introduce TSI buffers at the column pair level, as the distribution of the TSI looked rather marginal otherwise (risetime could degrade to 7-8ns).
- A new CMOS sense amp design has been done, and layed out. It uses relatively wide input transistors in the diff-amp input to achieve the low input impedance which keeps the voltage swings on the data bus very small.
- Simulations of a complete column pair, including these new designs, and annotated with the expected parasitics on the long busses, have been performed. The CEU buffers have been appropriately sized (TSI buffers are 32xMin, CEU control signals are 16-24xMin). The design seems to work well, but we are still awaiting more corner model information from Honeywell.
- Sense amp layout:



- First attempt at floorplanning for CEU region:



- Reserve about 150µ of vertical space for routing necessary horizontal busses across chip.
- Present layout uses only M2 for vertical bussing, leaving M1 and poly for horizontal bussing.
- Re-mapping of bits into the correct locations in the EOC buffers can be easily done below sense amps because of the extra routing layer.
- Blocks for senseamps, TSI buffers, CEU buffers, and CEU logic are shown in possible locations. Wiring to be done soon.

- Circuitry requires about 200µ vertically and 400µ horizontally, which is significantly smaller than in FE-D, despite addition of TSI buffers.
- Design still looks on target to achieve 600µ column-pair pitch.

End of Column Logic:

- Roberto has now been working on this for several weeks. He has done layout work for the RAM and CAM cells (the basic storage cells), which are somewhat smaller than in FE-D.
- He has been studying the design of the EOC logic in detail, trying to improve the design. He studied a fully static implementation of the comparator blocks in the CAM cells, but concluded there were no significant advantages in speed or robustness, and the present design is very compact and very fast.
- He is presently trying to finalize the design of the EOC logic, making some small improvements over the FE-D version. Layout will take another few weeks.

Peripheral Digital Logic:

- This is being handled by Gerrit, who will discuss progress in a separate talk.

Floorplanning:

- First serious discussions took place in LBL in April when Gerrit visited for one week.
- We presently believe that the FE-D floorplan is also a good model for FE-H. In particular, this means placing the relatively large DAC blocks of the current design below the EOC buffers, in a region where analog power bussing would be done.
- For a 3-metal chip, the present vertical channels between EOC buffers can be largely replaced by routing the digital lines directly over the EOC buffers in M3. A small routing channel between EOC blocks would be retained for bring DAC outputs from the bottom of the chip up to the bias cells under the analog column pairs.
- These discussions will be continued, at greater length, next week in the FE-H workshop.